Amendments ot the Specification:

Please replace paragraph number twenty (20) with the following amended paragraph:

Code Division Multiple Access CDMA is cellular technology that competes with GSM technology for dominance in the cellular world. XDSL ~~irefers~~ refers collectively to all types of digital subscriber lines, the two main categories being ADSL and SDSL. Two other types of xDSL technologies are High-data-rate DSL (HDSL) and Very high DSL (VDSL).

Please replace paragraph number thirty-six (36) with the following amended paragraph:

The output data of module **300** block is combined into a group of k-bits operating at a speed rate of fd fed into module **400** where I and Q are generated from a pre-selected constellation. The constellation is determined by the transmitted bit rate, available radio spectrum and the desired signal to noise ratio. The constellation selection is a compromise between radio bandwidth and acceptable bit error rate. The higher the constellation or larger the M-QAM selected, the smaller the radio bandwidth but higher the bit error rate. Once the selected constellation is determined, the I-bits and Q-bits are generated from the incoming k-bits group such that the combination of

all I and Q bits will generate M-QAM constellation points. Since, it is known a priori what each constellation point waveform should be, the calculated results can be stored in LUTs and the I-bits and Q-bits can be used to generate the right point. Taking advantage of the inherent LUTs and Adders and Registers in a FPGA device, the desired waveform of each constellation point can be parallel accessed to reduced the FPGA processing speed. The Nyquist rule dictates that the digital frequency should be at least 2 times the analog frequency. For practical applications, this number is usually

4. LUTs **800** to **803** store all possible waveforms of cosine and LUTs **820** to **823** store all possible waveform of sine. There are 4 LUTs tables for cosine and 4 LUTs for sine due to the reason explained above. Thus the output of the LUTs will generated a digitally modulated sine and cosine waveform and adders following the LUTs combine the sine and cosine into a digitally modulated QAM signal. The adders are shown in **113**, **114**, **115** and **116**. The registers ~~**126 to 128**~~ **124 to 127** that follow the adders are provided to digitally repeat the constellation point. The multiplexers **128** to **129** are also used to output the parallel digital samples into the DAC (Digital to Analog Converter) in serial format at a final clock rate of fs=fcL, where fc is the output carrier frequency and L is the upsampling selection. Without using the present scheme, the FPGA device processing speed would have to be fs instead of fd. For high output frequency and high upsampling, the ratio fs/fd could be 10 or higher. The reduction in logic speed improves performance of the FPGA device and reduces cost.